## ABSTRACT OF THE DISCLOSURE

A memory device is so adapted that data processing time is not prolonged even when there is little bus width. A DRAM is connected to first to third buffer circuits by buses, which have a bus width of 128 bits, via a selector. The first to third buffer circuits are connected to a circuit such as a signal processing circuit by buses having a bit width of 32 bits. Since part of the circuitry is connected by buses having a bit width of 32 bits, the wiring is simple. By executing various processing in parallel, it is possible to prevent prolongation of the time required to record image data on a memory card.